Claims

[c1] 1. A structure of a flash memory device, comprising:

a first conductive type substrate, which comprises a trench;

a second conductive type first well region located in the first conductive type substrate;

a stacked gate structure disposed on the first conductive type substrate;

a first spacer and a second spacer disposed on a sidewall of the stacked gate structure, wherein the first spacer connects with a top of the trench;

a source region located in the first conductive type substrate under the first spacer;

a drain region located in the first conductive type substrate under the second spacer;

a first conductive type second well region located between the stacked gate structure and the second conductive type first well region, wherein a junction between the first conductive type second well region and the second conductive type first well region is higher than a bottom of the trench;

a doped region located at the bottom and the sidewall of the trench, wherein the doped region is connected to the source region and makes the first conductive type second well isolated; and

a first contact located in the first conductive type substrate, wherein the first contact fills the trench and electrically connects with the source region and the first contact is isolated from the first conductive type second well region via the doped region.

[c2] 2. The structure of claim 1, wherein the first conductive type substrate includes a P-type substrate.

[c3] 3. The structure of claim 1, wherein the second conductive type first well region includes an N-type well region.

[c4] 4. The structure of claim 1, wherein the first conductive type second well region includes a P-type well region.

[c5] 5. The structure of claim 1, wherein the source region and the drain region are doped with N-type dopants.

[c6] 6. The structure of claim 1, wherein the drain region and the first conductive type second well region are short-circuited.

[c7] 7. The structure of claim 1, wherein the drain region and the first conductive type second well region are short-circuited by a second contact penetrating through a junction between the drain region and the first conductive type second well region.

[c8] 8. The structure of claim 17, wherein the structure further comprises:
an interlayer dielectric layer disposed on athe first conductive type substrate;
a plug disposed in the interlayer dielectric layer and electrically connected with the second contact; and
a conductive line disposed on the interlayer dielectric layer and electrically connected with the plug.

[c9] 9. The structure of claim 1, wherein the dopants of the doped region, the source region and the drain region are the same.

[c10] 10. A fabrication method for a flash memory device, comprising:
providing a first conductive type substrate, wherein the substrate comprises a second conductive type first well region, a first conductive type second well region and a stacked gate structure which are sequentially formed thereon;
forming a source region and a drain region in the substrate beside two sides of the stacked gate structure;
forming a spacer on a sidewll of the stacked gate structure;
forming a first patterned photoresist layer on the substrate, the first patterned photoresist layer exposes the substrate at the drain region;
etching the substrate at the drain region until penetrating through the junction between the drain region and the first conductive type second well region by using the first patterned photoresist layer and the stacked gate structure with the spacer as a mask;
removing the first patterned photoresist layer;
forming a second patterned photoresist layer on the substrate, the second patterned photoresist layer exposes the substrate at the source region;
etching the substrate at the source region to the second conductive type first

well region to form a trench by using the second patterned photoresist layer and the stacked gate structure with the spacer as a mask;
performing an ion implantation process to implant dopants at a bottom and a sidewll of the trench on the substrate to form a doped region;
removing the second patterned photoresist layer;
forming a first conductive layer on the substrate, wherein the first conductive layer fills a gap between the stacked gate structure;
removing a portion of the first conductive layer to form a first contact on the source region and a second conductive layer on the first conductive type second well region, wherein the first contact electrically connects with the source region and the doped region;
patterning the second conductive layer to form a second contact, wherein the drain region and the first conductive type second well region are short-circuited by the second contact;
forming an interlayer dielectric layer on the substrate; and
forming a conductive line on the interlayer dielectric layer, wherein the conductive line electrically connects with the second contact.

[c11] 11. The method of claim 10, wherein the ion implantation process includes a tilt angle ion implantation process.

[c12] 12. The method of claim 11, wherein a tilt angle for the ion implantation process is about 15 degrees to about 30 degrees.

[c13] 13. The method of claim 10, wherein the bottom of the trench and the sidewall of the trench form an obtuse angle.

[c14] 14. The method of claim 10, wherein the dopants of the ion implantation process, the source region and the drain region are the same.

[c15] 15. The method of claim 10, the method further comprising a step of forming a plug in the interlayer dielectric layer, wherein the plug electrically connects the conductive line and the second contact.

[c16] 16. The method of claim 10, wherein the first conductive type substrate includes a P-type substrate.

[c17] 17. The method of claim 10, wherein the second conductive type first well region includes an N-type well region.

[c18] 18. The method of claim 10, wherein the first conductive type second well region includes a P-type well region.

[c19] 19. The method of claim 10, wherein the step of removing the first conductive layer includes performing back etching.

[c20] 20. The method of claim 10, wherein the step of removing the first conductive layer includes performing chemical mechanical polishing